

MCR8DCM, MCR8DCN

Preferred Device

Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

Features

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Available in Surface Mount Lead Form – Case 369C
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- Pb-Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (T _J = -40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) MCR8DCM MCR8DCN	V _{DRM} , V _{RRM}	600 800	V
On-State RMS Current (180° Conduction Angles; T _C = 105°C)	I _{T(RMS)}	8.0	A
Average On-State Current (180° Conduction Angles; T _C = 105°C)	I _{T(AV)}	5.1	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, T _J = 125°C)	I _{TSM}	80	A
Circuit Fusing Consideration (t = 8.3 msec)	I ² t	26	A ² sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T _C = 105°C)	P _{GM}	5.0	W
Forward Average Gate Power (t = 8.3 msec, T _C = 105°C)	P _{G(AV)}	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec, T _C = 105°C)	I _{GM}	2.0	A
Operating Junction Temperature Range	T _J	-40 to 125	°C
Storage Temperature Range	T _{stg}	-40 to 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

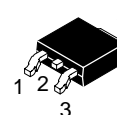
1. V_{DRM}, V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



ON Semiconductor®

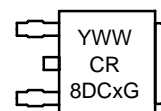
<http://onsemi.com>

SCRs
8 AMPERES RMS
600 – 800 VOLTS



DPAK
CASE 369C
STYLE 4

MARKING DIAGRAM



Y = Year
WW = Work Week
CR8DCx = Device Code
x = M or N
G = Pb-Free Package

PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

MCR8DCM, MCR8DCN

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction-to-Case – Junction-to-Ambient – Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.2 88 80	$^{\circ}\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes (Note 3)	T_L	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Peak Repetitive Forward or Peak Repetitive Reverse Blocking Current ($V_{AK} = \text{Rated } V_{DRM}$ or V_{RRM} , Gate Open)	I_{DRM} I_{RRM}	– –	– –	0.01 5.0	mA

ON CHARACTERISTICS

Peak On-State Voltage (Note 4) ($I_{TM} = 16 \text{ A}$)	V_{TM}	–	1.4	1.8	V
Gate Trigger Current (Continuous dc) ($V_{AK} = 12 \text{ V}$, $R_L = 100 \Omega$, $T_J = 25^{\circ}\text{C}$) ($T_J = -40^{\circ}\text{C}$)	I_{GT}	2.0 –	7.0 –	15 30	mA
Gate Trigger Voltage (Continuous dc) ($V_{AK} = 12 \text{ V}$, $R_L = 100 \Omega$, $T_J = 25^{\circ}\text{C}$) ($T_J = -40^{\circ}\text{C}$) ($T_J = 125^{\circ}\text{C}$)	V_{GT}	0.5 – 0.2	0.65 – –	1.0 2.0 –	V
Holding Current ($V_{AK} = 12 \text{ V}$, Initiating Current = 200 mA, Gate Open)	I_H	4.0 –	22 –	30 60	mA
Latching Current ($V_{AK} = 12 \text{ V}$, $I_G = 15 \text{ mA}$, $T_J = 25^{\circ}\text{C}$) ($V_{AK} = 12 \text{ V}$, $I_G = 30 \text{ mA}$, $T_J = -40^{\circ}\text{C}$)	I_L	4.0 –	22 –	30 60	mA

DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage ($V_{AK} = \text{Rated } V_{DRM}$, Exponential Waveform, Gate Open, $T_J = 125^{\circ}\text{C}$)	dv/dt	50	200	–	V/ μs
---	-------	----	-----	---	------------------

- Surface mounted on minimum recommended pad size.
- 1/8" from case for 10 seconds.
- Pulse Test: Pulse Width $\leq 2.0 \text{ ms}$, Duty Cycle $\leq 2\%$.

ORDERING INFORMATION

Device	Package	Shipping [†]
MCR8DCMT4	DPAK	2500 / Tape & Reel
MCR8DCMT4G	DPAK (Pb-Free)	
MCR8DCNT4	DPAK	
MCR8DCNT4G	DPAK (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MCR8DCM, MCR8DCN

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current

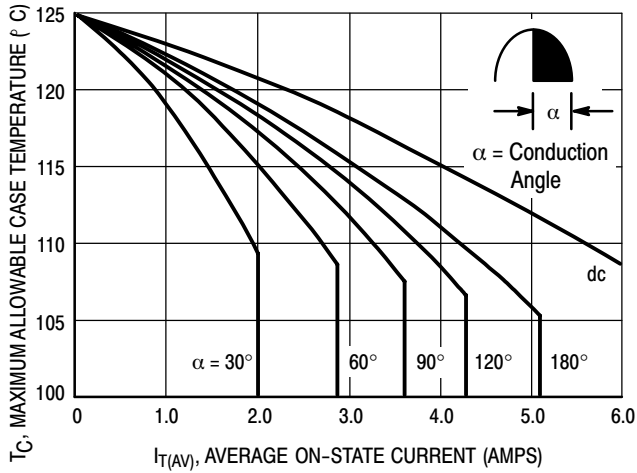
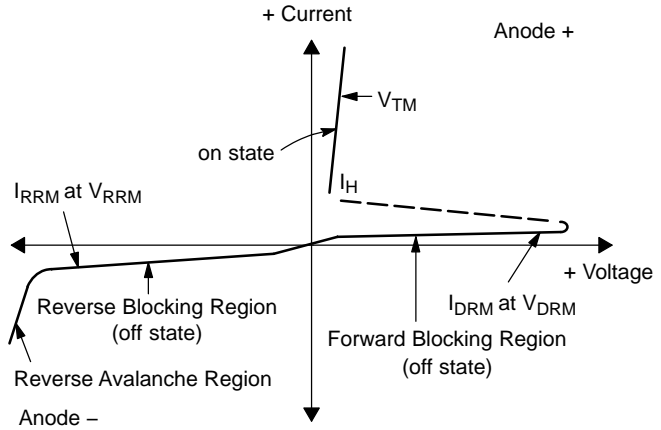


Figure 1. Average Current Derating

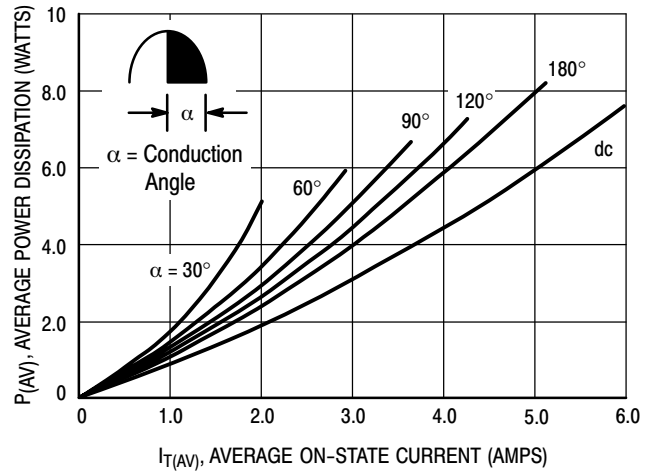


Figure 2. On-State Power Dissipation

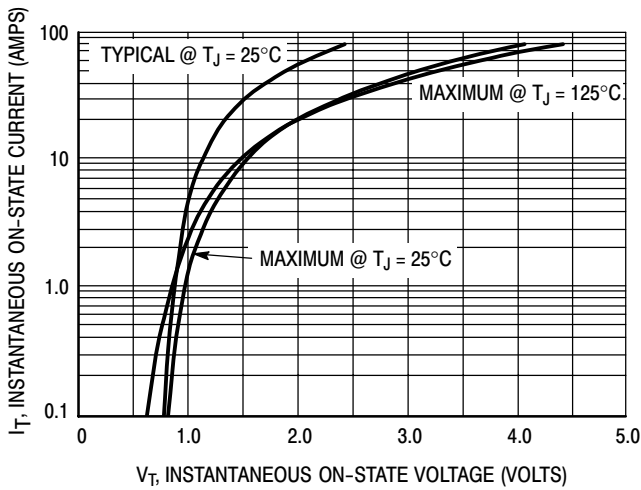


Figure 3. On-State Characteristics

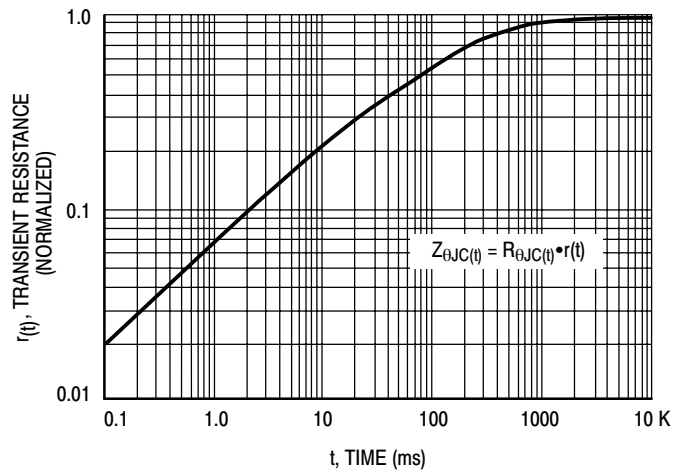


Figure 4. Transient Thermal Response

MCR8DCM, MCR8DCN

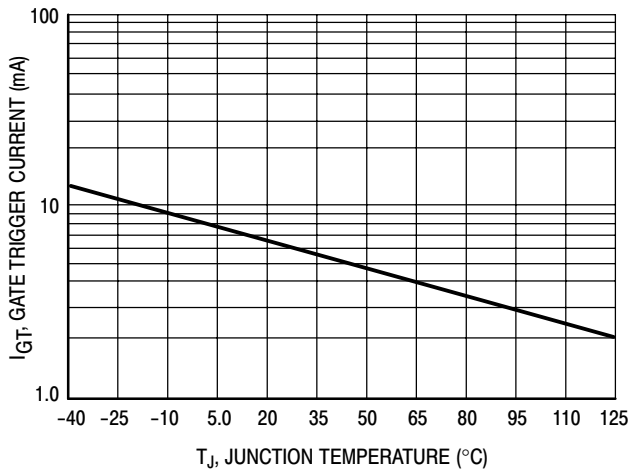


Figure 5. Typical Gate Trigger Current versus Junction Temperature

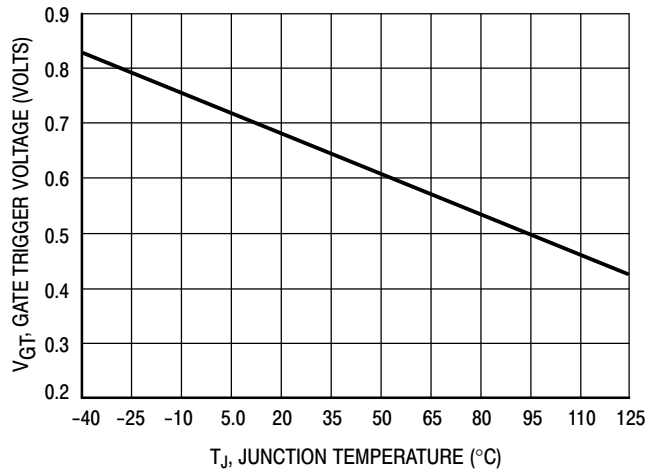


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

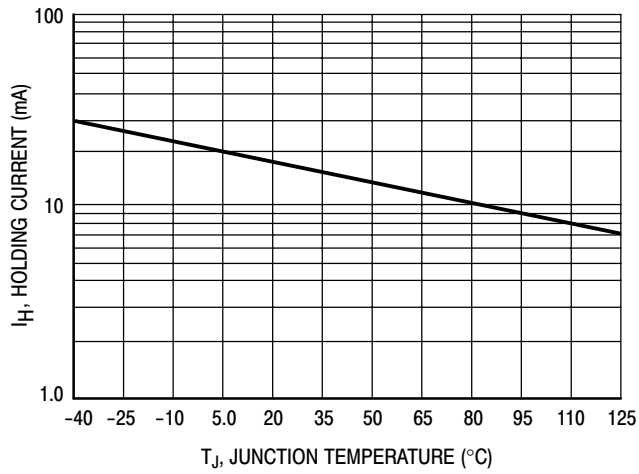


Figure 7. Typical Holding Current versus Junction Temperature

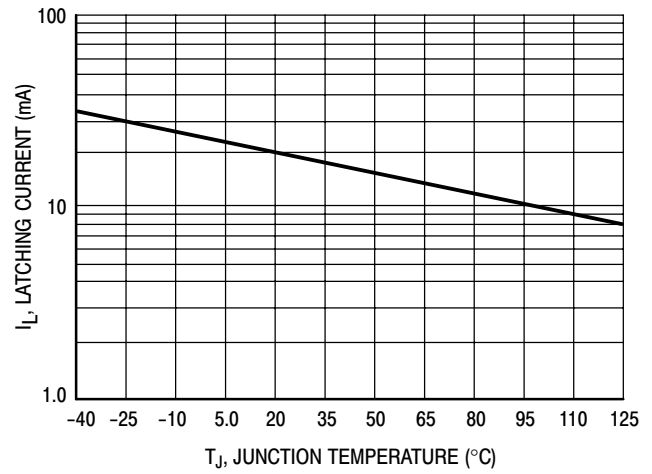


Figure 8. Typical Latching Current versus Junction Temperature

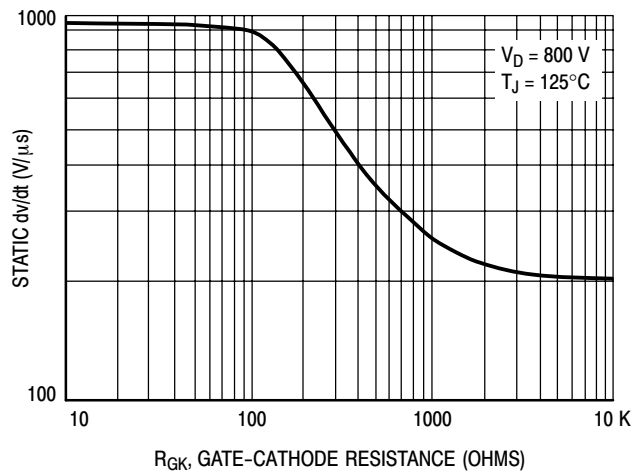
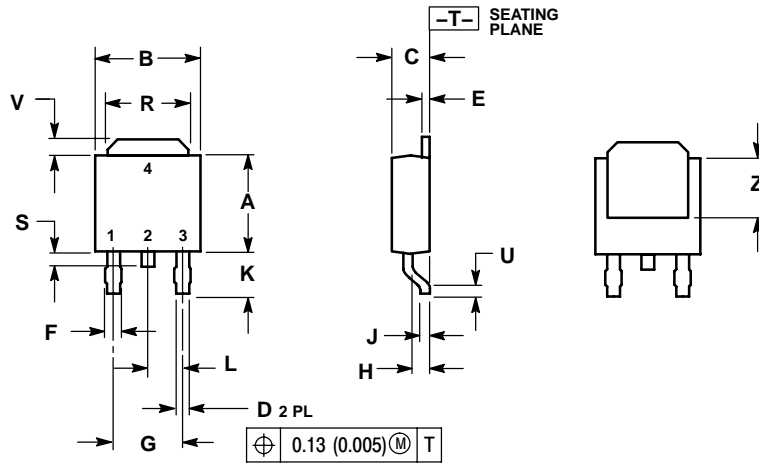


Figure 9. Exponential Static dv/dt versus Gate-Cathode Resistance

MCR8DCM, MCR8DCN

PACKAGE DIMENSIONS

DPAK CASE 369C ISSUE O

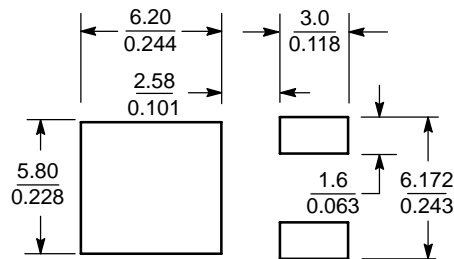


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.